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REMARKS

Claims 1-33 are currently pending in the subject application and are presently under consideration. A clean version of all pending claims is found at pages 2-7 of this Reply. No claims have been amended herein.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

II. Rejection of Claims 1-33 Under 35 U.S.C. §103(a)

Claims 1-33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Potter *et al.* (U.S. 6,157,393) in view of Aranda (U.S. 5,321,809). This rejection should be withdrawn for at least the following reasons. Neither Potter *et al.* nor Aranda, alone or in combination, teach or suggest each and every aspect set forth in the subject claims.

To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) *must teach or suggest all the claim limitations*. See MPEP §706.02(j). The *teaching or suggestion to make the claimed combination* and the reasonable expectation of success *must both be found in the prior art and not based on applicant's disclosure*. See *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The present invention relates generally to the field of video displays and more particularly to an improved raster engine with a multiple color depth digital display interface. Independent claim 1 recites "A raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays, comprising: at least one *control register programmable via the computer system to select a display mode*; a dual port RAM device operative to obtain pixel data from the frame buffer; and a logic device

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having a parallel output, the logic device being *adapted to select appropriate pixel data* from the dual port RAM device according to the selected display mode, *to remap the selected pixel data according to the selected display mode*, and to provide remapped selected pixel data at the parallel output according to a universal routing scheme applicable to the plurality of disparate displays.” Independent claims 20, 26, and 30 recite similar aspects. “Disparate” is defined as “markedly distinct in quality or character.” The raster engine of the subject claims “is easily programmed to interface a computer system running a variety of application programs with a plurality of disparate display types. The invention can thus be employed in high end as well as highly cost sensitive computer system applications in association with displays ranging from high definition television (HDTV) to low resolution monochrome EL and/or LCD display panels.” (Page 4, lines 26-31.) The raster engine of the subject claims is capable of selecting a display mode. (See, e.g., Claims 1, 21, 26, and 30.) “In addition, the raster engine can further comprise an integrated digital to analog converter (DAC) to support analog LCD displays and CRTs.” (Page 9, lines 13-14.) Furthermore, “[p]rogrammable compare and register logic 4 allows a user or a host system application program to select appropriate display modes for interfacing a frame buffer with one or a plurality of disparate display devices.” (Page 16, lines 23-25) Thus, the subject claims recite a system capable of selecting display modes for simultaneously displaying data on a variety of different types of (e.g. “disparate”) displays. Potter *et al.* does not teach or suggest these limitations of the subject claims.

The Examiner contends in the Advisory Action that the “plurality of disparate displays” has not been given patentable weight because the recitation occurs in the preamble, which is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness. Applicant’s representative respectfully points out that “a plurality of disparate displays” that is mentioned in the preamble of claim 1 is antecedent basis for “*the* plurality of disparate displays” referred to in the last line of claim 1, which receives remapped pixel data from a logic device having a parallel output. Thus, the body of claim 1 depends on the preamble for

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completeness (e.g., for antecedent basis), and claim 1 recites outputting remapped selected pixel data to a plurality (e.g., more than one) of disparate display devices.

As stated in the reply to Final Office Action Dated June 2, 2003, Potter *et al.* merely describes a system that directs graphical data to a display device 170. Contrary to the Examiner's assertion, the "bus controller 125...provided for controlling a bus 130" (Column 5, lines 66-67) does not teach or suggest the limitation of a control register able to *select or indicate a display mode*. Furthermore, according to Potter *et al.*, "The display device 170 preferably is a conventional horizontal scan cathode ray tube ("CRT") monitor having a plurality of pixels." (Column 6, lines 30-32.) Potter *et al.* discusses displaying data across two or more display devices. (See, e.g., Column 14, lines 28-34.) However, such display of data is merely a *single set of data* that is *formatted in a single predetermined manner* and divided for display on more than one display device. The referenced discussion of plural display devices does not teach or suggest a system capable of *formatting data* in a manner suitable for rendering on a *plurality of disparate display device types*. Thus, Potter *et al.* fails to teach or suggest all of the claim limitations of the subject application as recited in independent claims 1, 21, 26, and 30.

Aranda fails to make up for the aforementioned deficiencies of Potter *et al.* Aranda's discussion of a display interface states: "The display interface operates to generate the analog signals RGB on line 21 necessary to display the image on a display device (or CRT) 16 (along with the appropriate control signals). Although a CRT or monitor device is shown in the preferred embodiment, the techniques employed herein work equally well for *any two-dimensional display device* such as a plotter, printer, or other monitor type." (Column 5, lines 16-23, emphasis added.) Thus, Aranda merely discloses displaying data on a *single type* of display device at any single given time, as shown by the above-emphasized language. Aranda does not teach or suggest selecting display modes for simultaneously displaying data on a plurality of *disparate* devices.

To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the

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inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 149 F.3d 1350, 1357.

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

Moreover, Aranda *teaches away* from several aspects of the present invention. Specifically, Aranda discusses the *impracticability* of separating the frame buffer into two separate devices. The Examiner has stated that "it would have been obvious to combine the teaching of Aranda to the system of Potter because doing so would have *enabled* dividing the entire frame buffer into two separate devices so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices as noted in Aranda (col. 1, line 15 to col. 2, line 33)." Applicants respectfully point out that Aranda actually states, "The most straightforward approach to improving performance is to *divide the entire frame buffer into two separate devices* so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices." (col. 2, lines 22-26) (emphasis added). But, more importantly, Aranda then states, "The *difficulty with this approach*, however, is that twice the number of pins are required of the raster engine to access the dual devices. This requirement proves in practice to be a *significant complication*." (col. 2, lines 28-32) (emphasis added). Thus, Aranda actually *teaches away from* utilizing this approach, and combining Aranda with Potter could not enable a system that divides the frame buffer into two separate devices, let alone utilizes a dual port RAM, as found in the present invention.

In view of the above comments, it is readily apparent that neither Potter *et al.* nor Aranda, alone or in combination, teach or suggest the presently claimed invention as recited in independent claims 1, 21, 26, and 30 and claims 2-20, 22-25, 27-29, and 31-33, which depend respectively there from. This rejection should be withdrawn.

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CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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